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EXAMINER

PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
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2841

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/685,042

Applicant(s)

CAMERLO ET AL.

Examiner

Ishwar (I. B.) Patel

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 October 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 20-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/7/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C.

121:

- I. Claims 1-19, drawn to a printed circuit board, classified in class 174, subclass 255.
- II. Claims 20-24, drawn to a method of fabricating a circuit board, classified in class 29, subclass 830+.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions group II and group I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process. The circuit board does not need the steps of providing the pad layout. The circuit board can be manufactured with a previously known layout structure.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different

Art Unit: 2841

classification, and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with David E. Huang (Reg. 39,229) on April 25, 2005 a provisional election was made without traverse to prosecute the invention of a printed circuit board, claims 1-19. Affirmation of this election must be made by applicant in replying to this Office action. Claims 20-24 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 8-9, 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Natarajan et al., (US Patent No. 5,519,580).

Regarding claim 1, Natarajan et al., in figure 2, discloses a pad layout for mounting with a circuit board component, the pad layout comprising: a set of pads (set of pads as marked on figure 2 in appendix "A") arranged on a surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction (see figure 2), each pad of the set of pads having (i) a central portion (28, as shown in figure 3 in detail) and (ii) multiple lobe portions (26, as shown in detail in figure 3) integrated with the central portion (28) and extending from the central portion of that pad (see figure 3).

Regarding claim 2, Natarajan et al., further discloses for each pad of the set of pads, that pad has exactly four lobe portions that extend from the central portion of that pad.

Regarding claim 3, Natarajan et al., further discloses for each pad of the set of pads, two of the four lobe portions of that pad extend along a first axis, and another two of the four lobe portions of that pad extend along a second axis that is substantially perpendicular to the first axis (see figure 3, two of the lobes are extend along one (first) axis and the other to extend perpendicular to the first axis).

Regarding claim 8, Natarajan et al., further discloses each pad of the set of the pads substantially has: a first length along a first axis (axis passing between two of the lobes and length along that axis) and the first length along a second axis (axis perpendicular to the first axis and length along that axis) that is substantially perpendicular to the first axis, and a second length along a third axis (second length along the axis passing through the lob) and the second length along a fourth axis (second length along the axis perpendicular to the third axis) that is substantially perpendicular to the third axis, and wherein the second length is greater than the first length (length along the lobe is greater than that of the length along the axis not passing through the lobe, see figure 3).

Regarding claim 9, Natarajan et al., further discloses the first and second axes are pivoted from the third and fourth axes by substantially 45 degrees (axis passing through the lobes is pivoted by 45 degrees than that of not passing through the lobes).

Regarding claim 11, Natarajan et al., in figure 2, discloses a circuit board, comprising: a set of circuit board layers (set of circuit board layers not shown in figure but the structure of package 10 is with internal routing wires in different layers, column 2, line 53-56) combined to form a rigid planar structure having an outer surface (16); and a pad layout (layout as shown in figure 2) configured to mount with a circuit board component, the pad layout (pad layout as shown in

Art Unit: 2841

figure 2) including a set of pads (set of pads as marked on figure 2 in appendix "A"), arranged on the surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction (see marked up figure 2 in appendix "A"), each pad of the set of pads having (i) a central portion (28, as shown in figure 3 in detail) and (ii) multiple lobe portions (26, as shown in detail in figure 3) integrated with the central portion and extending from the central portion of that pad.

Regarding claim 12, Natarajan et al., further discloses for each pad of the set of pads, that pad has exactly four lobe portions (26, as shown in detail in figure 3) that extend from the central portion (28) of that pad, two of the four lobe portions of that pad extending along a first axis (axis passing from two of the lobe portions), and another two of the four lobe portions of that pad extending along a second axis (axis passing through the other of the four lobe portions) that is substantially perpendicular to the first axis.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2841

9. Claims 4, 5, 10, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Natarajan et al., (US Patent No. 5,519,580), as applied to claim 1 above, and further in view of Darveaux et al., US Patent No. 6,201,305.

Regarding claim 4, Natarajan et al., discloses all the features of the claimed invention as applied to claim 1 above, including each pad of the set of pads has a profile having multiple outer radii as shown in detail in figure 3, but does not disclose the multiple outer radii of substantially 3 mils.

Darveaux et al., discloses pads with multiple outer radii as shown in figure 3A and 4A and further recites that the central pad and lobes (spokes 32) can vary widely depending upon the particular application at hand (column 6, line 32-42), to have better shear performance, ball thermal cycle reliability, ball attach yield, and ball positional tolerance (column 4, line 28-34).

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the pads with profile having multiple outer radii of substantially 3 mils, as taught by Darveaux et al., in order to have better shear performance, ball thermal cycle reliability, ball attach yield, and ball positional tolerance.

Regarding claim 5, Natarajan et al., discloses all the features of the claimed invention as applied to claim 4 above, but does not disclose the profile of each pad of the set of pads further has multiple concave radii of substantially 8 mils.

Darveaux et al., discloses pads with multiple out radii and multiple concave radii, as shown in figure 3A and 4A and further recites that the central pad and lobes (spokes 32) can vary widely depending upon the particular application at hand (column 6, line 32-42), to have better shear performance, ball thermal cycle reliability, ball attach yield, and ball positional tolerance (column 4, line 28-34).

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide each pad with profile having multiple concave radii of substantially 8 mils, as taught by Darveaux et al., in order to have better shear performance, ball thermal cycle reliability, ball attach yield, and ball positional tolerance.

Regarding claim 10, Natarajan et al., discloses all the features of the claimed invention as applied to claim 8 above, but does not disclose the first length is substantially 18 mils and the second length is substantially 24 mils.

Art Unit: 2841

Darveaux et al., discloses pads with multiple outer radii and multiple concave radii, as shown in figure 3A and 4A and further recites that the central pad and lobes (spokes 32) can vary widely depending upon the particular application at hand (column 6, line 32-42), to have better shear performance, ball thermal cycle reliability, ball attach yield, and ball positional tolerance (column 4, line 28-34).

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide pads of Natarajan et al., with the first length substantially 18 mils and the second length is substantially 24 mils, as taught by Darveaux et al., in order to have better shear performance, ball thermal cycle reliability, ball attach yield, and ball positional tolerance.

Regarding claim 13, Natarajan et al., discloses all the features of the claimed invention as applied to claim 11 above, but does not disclose each pad of the set of pads has a profile having multiple outer radii of substantially 3 mils, and multiple concave radii of substantially 8 mils.

Darveaux et al., discloses pads with multiple outer radii and multiple concave radii, as shown in figure 3A and 4A and further recites that the central pad and lobes (spokes 32) can vary widely depending upon the particular application at hand (column 6, line 32-42), to have better shear performance, ball

Art Unit: 2841

thermal cycle reliability, ball attach yield, and ball positional tolerance (column 4, line 28-34).

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide pads of Natarajan et al., with each pad of the set of pads has a profile having multiple outer radii of substantially 3 mils, and multiple concave radii of substantially 8 mils, as taught by Darveaux et al., in order to have better shear performance, ball thermal cycle reliability, ball attach yield, and ball positional tolerance.

Regarding claim 15, Natarajan et al., discloses all the features of the claimed invention as applied to claim 11 above, including each pad of the set of pads substantially has: a first length along a first axis (axis passing between two of the lobes and length along that axis) and the first length along a second axis (axis perpendicular to the first axis and length along that axis) that is substantially perpendicular to the first axis, and a second length along a third axis (second length along the axis passing through the lob) and the second length along a fourth axis (second length along the axis perpendicular to the third axis) that is substantially perpendicular to the third axis; and wherein the first and second axes are pivoted from the third and fourth axes by substantially 45 degrees (axis passing through the lobes is pivoted by 45 degrees than that of not passing

Art Unit: 2841

through the lobes), but does not disclose **the first length is substantially 18 mils, and wherein the second length is substantially 24 mils.**

Darveaux et al., discloses pads with multiple outer radii and multiple concave radii, as shown in figure 3A and 4A and further recites that the central pad and lobes (spokes 32) can vary widely depending upon the particular application at hand (column 6, line 32-42), to have better shear performance, ball thermal cycle reliability, ball attach yield, and ball positional tolerance (column 4, line 28-34).

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide pads of Natarajan et al., with the first length substantially 18 mils and the second length is substantially 24 mils, as taught by Darveaux et al., in order to have better shear performance, ball thermal cycle reliability, ball attach yield, and ball positional tolerance.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Natarajan et al., (US Patent No. 5,519,580), as applied to claim 1 above, and further in view Wu, (US Patent Application Publication No. 2002/0071935).

Regarding claim 6, Natarajan et al., discloses all the features of the claimed invention as applied to claim 1 above, including solder mask (32) on the

Art Unit: 2841

surface of the circuit board, having a central aperture portion but does not disclose the solder mask having multiple lobe aperture portions integrated with the central aperture portion to mirror a profile of a corresponding pad.

Natarajan et al., discloses mask with aperture which fully exposes the central portion of corresponding pad and partly covering the lobe portion of the corresponding pad, (figure 3).

Wu, in figure 6A and 8, discloses a non solder mask defined pad structure with mask having central aperture and further having multiple lobe aperture portions (ditch like grooves) integrated with the central aperture portion to mirror a profile of a corresponding pad. Wu further recites that because of such design, the contact area between the solder paste and solder pad is expanded. Hence when doing the reflow process, the adhesion force will be greatly increased (page 1, paragraph 0008).

A person of ordinary skill in the art at the time of applicant's invention would have recognized the advantage of providing non solder mask defined pad structure with the solder mask having multiple lobe aperture portions in order to increase the contact area between the solder paste and solder pad to increase the adhesion force during solder reflow process.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the solder mask around the pad of Natarajan et al., having multiple lobe aperture portions integrated with the central aperture portion to mirror a profile of a corresponding pad, as taught by

Art Unit: 2841

Wu, in order to increase the contact area between the solder paste and solder pad to increase the adhesion force during solder reflow process.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over modified pad layout of Natarajan et al., (in combination with Wu), as applied to claim 6 above, and further in view of Fukasawa, (US Patent No. 5,844,782).

Regarding claim 7, Natarajan et al., discloses all the features of the claimed invention including the clearance regions defined by the solder mask as applied to claim 6 above, but does not disclose clearance regions are substantially 2 mils wide around each pad of the set of pads.

Fukasawa, in figure 3A, discloses a solder mask (pattern protecting film 17) around the pad having a clearance of about 2 mils (gap of 0.05 mm, column 3, line 30) and further recites that "(e)ven when a temperature cycles test or the like is carried out, the external electrode 13 and the pattern protecting film 17, the thermal expansion coefficients of which are greatly different, are kept out of contact with each other and consequently thermal stresses do not act in the base portions of the external electrodes 13 as has happened in devices of the related art of this kind".

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Art Unit: 2841

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified solder mask opening of the Natarajan et al., with a clearance regions substantially 2 mils wide around each pad of the set of pads, as taught by Fukasawa, in order to avoid contacting the mask to the solder on the pad causing thermal stresses.

12. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over circuit board of Natarajan et al., as applied to claim 11 above, and further in view of Wu, (US Patent Application Publication No. 2002/0071935) and Fukasawa, (US Patent No. 5,844,782).

Regarding claim 14, Natarajan et al., discloses all the features of the claimed invention as applied to claim 11 above, including solder mask (32) on the surface of the circuit board, having a central aperture portion but does not disclose **the solder mask having multiple lobe aperture portions integrated with the central aperture portion to mirror a profile of a corresponding pad and the solder mask further defining clearance regions that are substantially 2 mils wide around each pad of the set of pads.**

Natarajan et al., discloses mask with aperture which fully exposes the central portion of corresponding pad and partly covering the lobe portion of the corresponding pad, (figure 3).

Wu, in figure 6A and 8, discloses a non solder mask defined pad structure with mask having central aperture and further having multiple lobe aperture portions (ditch like groove) integrated with the central aperture portion to mirror a

Art Unit: 2841

profile of a corresponding pad. Wu further recites that because of such design, the contact area between the solder paste and solder pad is expanded. Hence when doing the reflow process, the adhesion force will be greatly increased (page 1, paragraph 0008).

A person of ordinary skill in the art at the time of applicant's invention would have recognized the advantage of providing non solder mask defined pad structure with the solder mask having multiple lobe aperture portions in order to increase the contact area between the solder paste and solder pad to increase the adhesion force during solder reflow process.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the solder mask around the pad of Natarajan et al., having multiple lobe aperture portions integrated with the central aperture portion to mirror a profile of a corresponding pad, as taught by Wu, in order to increase the contact area between the solder paste and solder pad to increase the adhesion force during solder reflow process.

Further, Fukasawa, in figure 3A, discloses a solder mask (pattern protecting film 17) around the pad having a clearance of about 2 mils (gap of 0.05 mm, column 3, line 30) and further recites that "(e)ven when a temperature cycles test or the like is carried out, the external electrode 13 and the pattern protecting film 17, the thermal expansion coefficients of which are greatly different, are kept out of contact with each other and consequently thermal stresses do not act in the base portions of the eternal electrodes 13 as has happened in devices of the related art of this kind".

Art Unit: 2841

Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified solder mask opening of the Natarajan et al., with a clearance regions substantially 2 mils wide around each pad of the set of pads, as taught by Fukasawa, in order to avoid contacting the mask to the solder on the pad causing thermal stresses.

13. Claims 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forehand et al., US Patent No. 5,847,936 in view of Natarajan et al., (US Patent No. 5,519,580).

Regarding claim 16, Forehand et al., in figure 3, discloses a circuit board assembly, comprising: a set of circuit board layers (231-235) combined to form a rigid planar structure (printed circuit board 220) having an outer surface (outer surface of the board); a pad layout (pad layout as shown in figure 5) including a set of pads arranged on the surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction (pad pattern 401, shown in detail in figure 5), a circuit board component (integrated circuit 201, column 2, line 45-50) mounted to the pad layout via a set of solder joints (219).

Art Unit: 2841

Forehand et al., does not disclose each pad of the set of pads having (i) a central portion (26, as shown in detail in figure 3) and (ii) multiple lobe portions (26, as shown in detail in figure 3) integrated with the central portion and extending from the central portion of that pad.

Natarajan et al., in figure 1 discloses a package substrate with pad layout (shown in detail in figure 2) and further discloses pads having (i) a central portion (26, as shown in detail in figure 3) and (ii) multiple lobe portions (26, as shown in detail in figure 3) integrated with the central portion and extending from the central portion of that pad, in order to have an uniform and robust solder joints (column 1, line 50).

A person of ordinary skill in the art would have recognized the advantages of providing lobes on the pad in order to have uniform and robust solder joints.

Therefore, it would have been obvious to a person of ordinary skill in the art to modify the pads structure of the circuit board of Forehand et al., to have lobes as taught by Natarajan et al., in order to have an uniform and robust solder joints.

Regarding claim 18, the modified circuit board assembly of Forehand et al., further discloses the circuit board component includes ball grid array package having a set of ball-shaped (219) contacts corresponding to the set of pads.

Regarding claim 19, Forehand et al., in figure 3, discloses a circuit board assembly, comprising: a set of circuit board layers (231-235) combined to form a

Art Unit: 2841

rigid planar structure (printed circuit board 220) having an outer surface (outer surface of the board); a pad layout (pad layout as shown in figure 5) including a set of pads arranged on the surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction (pad pattern 401, shown in detail in figure 5), a circuit board component (integrated circuit 201, column 2, line 45-50), means (solder ball 219) for mounting the circuit board component to the set of pads of the pad layout.

Forehand et al., does not disclose each pad of the set of pads having (i) a central portion (26, as shown in detail in figure 3) and (ii) multiple lobe portions (26, as shown in detail in figure 3) integrated with the central portion and extending from the central portion of that pad.

Natarajan et al., in figure 1 discloses a package substrate with pad layout (shown in detail in figure 2) and further discloses pads having (i) a central portion (26, as shown in detail in figure 3) and (ii) multiple lobe portions (26, as shown in detail in figure 3) integrated with the central portion and extending from the central portion of that pad, in order to have an uniform and robust solder joints (column 1, line 50).

A person of ordinary skill in the art would have recognized the advantages of providing lobes on the pad in order to have uniform and robust solder joints.

Therefore, it would have been obvious to a person of ordinary skill in the art to modify the pads structure of the circuit board of Forehand et al., to have

Art Unit: 2841

lobes as taught by Natarajan et al., in order to have an uniform and robust solder joints.

14. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the modified circuit board assembly of Forehand et al., (in combination of Natarajan et al.) as applied to claim 16 above, and further in view of Katchmar, US Patent No. 6,194,782.

Regarding claim 17, the modified circuit board assembly of Forehand et al., discloses all the feature of the claimed invention as applied to claim 16 above, but does not disclose the circuit board component includes a ceramic column grid array package having a set of column-shaped contacts corresponding to the set of pads.

Katchmar discloses that integrated circuit packages to area array packages, both the ball grid array package (as shown in figure 4, 5 and 6) and ceramic column grid array package (as shown in figure 7) installed on circuit board (substrate 28), are known in the art, in order to have large number of interconnection between the package and the substrate, column 1, line 5-24.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board assembly of Forehand et al., with the circuit board component including a ceramic column grid array package having a set of column-shaped contacts corresponding to the set of pads, as taught by Katchmar, in order to have desired large number of interconnection between the package and the substrate.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Burnette et al, in figure 4, discloses both solder mask defined (SMD) and non solder mask defined (NMSD, with clearance around pad) and recites the advantages of good thermal cycling reliability and good bending reliability can be achieved for the same printed circuit board by including both SMD and NMSD bonding pads on the same semiconductor device (column 2, line 46-50).

Takigami, US Patent No. 6,218,630, in figure 4, a pad layout structure with discloses solder mask having clearance around the pads.

Lee, US Patent No. 5,872,399, in figure 6A, discloses a pad structure with multiple lobes extended from the central portion of the pad.

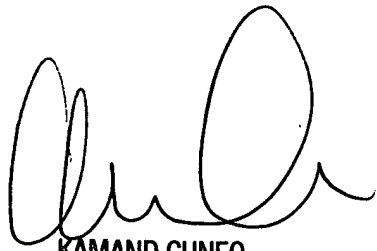
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2841

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
April 29, 20



KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800